between about 10 MHz to 15GHz. A circuit board for electronic parts is also provided including a plate-like ground layer, an insulating substrate disposed on the plate-like ground layer, a plurality of leads disposed on the insulating substrate, and a conductor disposed on an insulating material on the plurality of leads. The conductor disposed on the insulating material on the plurality of leads reduces a self inductance of the plurality of leads by flowing eddy current through the conductor and the insulating substrate disposed on the plate-like ground layer reduces a self inductance of the plurality of leads by flowing eddy current through the plate-like ground layer.

REMARKS

Claims 1 and 3-9 are presently pending.

The Office Action objected to the drawings, stating the figures are improperly cross-hatched and that "all of the parts in cross section, and only those parts, must be cross-hatched." Applicants request that the Examiner specifically identify the alleged impropriety. A review of the drawings reveals that only parts in cross section are cross-hatched. Further, where the meaning of the drawing would be obscured by cross-hatching, such as in Fig. 2, cross-hatching was omitted for clarity. Regarding selection of the cross-hatching based on the material of the part, Applicants are not required to select from those shown on page 600-84 of the MPEP, and the cross-hatching employed is sufficient, in combination with the specification, to clearly identify the materials and boundries thereof. If the Examiner has specific deficiencies or suggestions with regard to the drawings, the Examiner is invited to provide such information.

The Office Action also stated that in Figure 8, section B-B' should be section 9-9 to correspond to Figure 9. This matter is addressed in the amendments to the specification provided herein and the accompanying Drawing Change Authorization Request. The Drawing Change Authorization Request also requests approval for changes to correct spelling errors in Figs. 5, 19, and 20.

In accord with the above comments, withdrawal of the objection to the drawings is requested.

The Abstract was objected to as being too long and imprecise. The Abstract is amended herein to address this objection. Withdrawal of this objection is requested.

The Specification was objected to for not having legible page numbers. Provided herewith is a Substitute Specification. No changes have been made to the specification and, therefore, no new matter is introduced. The Substitute Specification is a formal copy of the specification intended to replace the poor facsimile copy of the specification as filed. The page numbers are clearly legible in the Substitute Specification. Withdrawal of the objection is therefore requested.

35 U.S.C. § 112 Rejection

Claims 1-2 and 5-9 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Claim 2 has been cancelled without prejudice or disclaimer. Claims 1, 5, and 6 have been amended. Therefore, it is believed that claims 1 and 5-9 are in full compliance with 35 U.S.C. § 112, second paragraph, and reconsideration and withdrawal of this rejection is requested in view of the enclosed amendments.

With respect to the Examiner's statement of the reason for rejection of claim 7 under 35 U.S.C. § 112, second paragraph, it is submitted that claim 7, as written,

complies fully with 35 U.S.C. § 112, second paragraph. Definiteness of claim language must be analyzed in light of the content of the application disclosure, the teachings of the prior art, and the claim interpretation that would be given by one of ordinary skill in the art at the time the invention was made. The essential inquiry is whether the claims set out and circumscribe a particular subject matter with a reasonable degree of clarity. Whether more suitable language or modes of expression are available in not the requisite test. The specification and Figures clearly describe and illustrate the relation between the insulating material (e.g., 6) and the adhesive layer (e.g., 9) (see, e.g., Figures 19-20 and corresponding text) sufficiently to enable one skilled in the art to understand the meaning of the term "contains" in claim 7. Thus, the term is sufficiently descriptive under 35 U.S.C. § 112, second paragraph, and withdrawal of the 35 U.S.C. § 112 rejection of claim 7 is requested.

35 U.S.C. § 102(b) Rejection over Anderson

Claims 1-2 and 5-6 were rejected under 35 U.S.C. § 102(b) as being anticipated by **Anderson** (U.S. Pat. No. 4,441,088). Reconsideration and withdrawal of this rejection is requested in view of the amendments herein and the remarks below.

Claim 1 provides a wiring board for a semiconductor device. This wiring board includes a wiring section disposed on an insulation board and an electromagnetic shielding film disposed at a position close to the wiring section. A distance defined between said wiring section and said electromagnetic shielding film is 150 μm or less and a volume specific resistance of said electromagnetic shielding film is 30 μΩ·cm or less at a room temperature. This structure provides, over an applicable frequency between about

10 MHz to 15GHz, a reduction in inductance of the wiring section and a reduction in inductive cross talk.

In accord with the claimed structure, the eddy current generated on the electromagnetic shielding film can be increased. The eddy current, which is generated by the current flowing through a plurality of leads on a wiring board, flows in a direction in which a magnetic flux is canceled. Therefore, inductances of the lines (self inductance as well as mutual inductance between leads) and inductive cross talk can be decreased, speeding up in transmission of signal and data can be achieved. These effects are significant and unexpected results of the present invention.

Anderson relates to planar transmission lines having reduced forward wave crosstalk (see, e.g., col. 1, lines 6-12; col. 2, lines 54-68) and comprises a plurality of leads in an insulator layer and a conductor provided on one surface of the insulator layer. **Anderson** does not disclose or suggest that a distance defined between the wiring section and the electromagnetic shielding film is 150 μm or less. **Anderson** also does not teach or suggest a volume specific resistance of a material of the electromagnetic shielding film is 30 μΩ·cm or less at a room temperature and that an objective range extends from around 10 MHz to 15 GHz in sinusoidal frequency. Therefore, **Anderson** does not anticipate claim 1.

Claims 5 and 6 provide a circuit board for electronic parts including a plate-like ground layer, an insulating substrate disposed on the plate-like ground layer, a plurality of leads disposed on the insulating substrate, and a conductor disposed on an insulating material on the plurality of leads. The conductor disposed on the insulating material on the plurality of leads reduces a self inductance of the plurality of leads by flowing eddy

current through the conductor and the insulating substrate disposed on the plate-like ground layer reduces a self inductance of the plurality of leads by flowing eddy current through the plate-like ground layer. **Anderson** does not teach or suggest both a plate-like ground layer and a conductor disposed on an insulating material on the plurality of leads, as claimed. Therefore, **Anderson** does not anticipate claims 5 and 6.

Thus, **Anderson** does not teach each and every element of the claimed invention and does not anticipate claims 1, 5 or 6 under 35 U.S.C. § 102(d). Withdrawal of this rejection is respectfully requested.

35 U.S.C. § 102(b) Rejection over Elliott

Claims 1-2 and 5-6 were rejected under 35 U.S.C. § 102(b) as being anticipated by **Elliott et al.** (U.S. Pat. No. 4,367,585). Reconsideration and withdrawal of this rejection is requested in view of the amendments herein and the remarks below.

It is alleged that **Elliott et al.** provide a board with a plurality of leads 14 on insulating material 16 and a conductor 13 on the leads.

Elliott et al. relate to flat, flexible cable used in the telecommunications industry in applications wherein the cable may be folded back on itself, such as "under-carpet cable" (see, e.g., col. 1, lines 15-25). As shown in Fig. 1, for example, **Elliott et al.** provide a flexible cable with two offset arrays of conductors 13, 14 separated by a thin, non-adhesive backed center plastic film 16, wherein the structure is laminated between outer films 18, 19. **Elliott et al.** particularly relate to a method of manufacturing this structure.

However, **Elliott et al.** do not teach or suggest that a distance defined between the wiring section and the electromagnetic shielding film is 150 μm or less. **Elliott et al.**

also do not teach or suggest a volume specific resistance of a material of the electromagnetic shielding film is 30 μΩ·cm or less at a room temperature and that an objective range extends from around 10 MHz to 15 GHz in sinusoidal frequency. Therefore, **Elliott et al.** do not anticipate claim 1.

With respect to claims 5 to 9, which require a circuit board for electronic parts including a plate-like ground layer, an insulating substrate disposed on the plate-like ground layer, a plurality of leads disposed on the insulating substrate, and a conductor disposed on an insulating material on the plurality of leads. **Elliott et al.** do not provide such structure. Moreover, as **Elliott et al.** do not provide a plate-like ground layer, **Elliott et al.** is unable to dispose an insulating substrate thereon to reduce a self inductance of the plurality of leads by flowing eddy current through the plate-like ground layer. Therefore, **Elliott et al.** do not anticipate claims 5 to 9 for at least these reasons.

35 U.S.C. § 103(a) Rejection over Kabadi

Claims 5 and 7-8 were rejected under 35 U.S.C. § 103(a) as being unpatentable over **Kabadi** (U.S. Pat. No. 4,798,918). Reconsideration and withdrawal of this rejection is requested in view of the amendments herein and the remarks below.

It is alleged **Kabadi** provides a plurality of leads 42, 35, 36 on an insulating material 54 and a conductor 32, 41, 33 disposed over the leads, wherein an adhesive 53 is contained on the insulating material on the side opposite the conductor.

Kabadi relates to high density electric cabling systems and provides a single layer flat cable having alternating signal and ground traces (see, e.g., col. 1, lines 6-20). The flexible circuit includes a plurality of ground traces 21, 22 and, interspersed between the

ground traces, a plurality of signal traces 24 (see, e.g., col. 2, lines 32-38). These traces are formed on both sides of polyimide strip 54.

Claims 5 and 7-8 require a circuit board for electronic parts including a plate-like ground layer, an insulating substrate disposed on the plate-like ground layer, a plurality of leads disposed on the insulating substrate, and a conductor disposed on an insulating material on the plurality of leads wherein the conductor disposed on the insulating material on the plurality of leads reduces a self inductance of the plurality of leads by flowing eddy current through the conductor and wherein the insulating substrate disposed on the plate-like ground layer reduces a self inductance of the plurality of leads by flowing eddy current through the plate-like ground layer.

Kabadi do not teach or suggest, for example, the claimed a plate-like ground layer which, in combination with the insulating substrate disposed thereon, reduces a self inductance of the plurality of leads by flowing eddy current through the plate-like ground layer. Instead, **Kabadi** provide a plurality of ground traces 21, 22 interspersed with signal traces 24. Thus, in **Kabadi's** structure, eddy currents are generated locally, along the lines of lead patterns, and provide only limited eddy current generation. On the other hand, in the present invention, the plate-like ground layer and insulative substrate combination provides generation of a large eddy current over the entire area of the plate-like ground layer. Further, claims 5 and 7-8 provide conductors deposited on the upper surfaces of the leads, as shown for example in Figure 19 of the present invention, sandwiching both the upper and lower surfaces of the leads by large eddy currents to decrease the self inductance of the leads and suppress noise.

Thus, **Kabadi** does not teach or suggest all of the elements of claims 5 or 7-8 and does not establish, in combination with the Examiner's allegations, a *prima facie* case of obviousness under 35 U.S.C. § 103(a) for at least the reasons asserted above.

If the Examiner has any questions or comments regarding this Amendment or application, she is kindly requested to contact the undersigned at the phone number listed below.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

William D. Pegg
Registration No. 42,988

600 13th Street, N.W.
Washington, DC 20005-3096
(202) 756-8000 WDP:lnm
Date: April 12, 2001
Facsimile: (202) 756-8087

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

Please replace lines 11 and 12 on page 7 with the following:

FIG. 9 is a sectional view taken along the line [B-B'] 9-9 of FIG. 8;

Please replace the first full paragraph on page 14 with the following rewritten paragraph:

--FIG. 7 is a schematic planar view showing an outlined constitution of a DRAM having BGA structure of CSP type according to the second preferred embodiment of the invention. FIG. 8 is an enlarged view showing the essential part of FIG. 7, FIG. 9 is a sectional view taken along the line [B-B'] 9-9 of FIG. 8, and FIG. 10 is a developed sectional view showing a detailed constitution of the electromagnetic shielding structure shown in FIG. 9. In FIGS. 7 to 10, inclusive, reference numeral 21 designates a semiconductor chip, 21A an external electrode (bonding pad) for the semiconductor chip 21, 22 an electromagnetic shielding film, 23 an insulating film (polyimide film), 31 a solder ball, 32 leads (copper foil wiring) in a package having BGA structure of CSP type, 33 a polyimide film (insulating film) after having worked a cavity for mounting solder ball, 34 an adhesive of epoxy or the like base resin, 35 a cavity for mounting solder ball, and 36 a thermoplastic adhesive prepared from thermoplastic polyimide or B-stage epoxy, respectively.--

IN THE CLAIMS:

Please cancel claim 2 without prejudice or disclaimer.

Please amend the claims as follows:

1. (Amended) A wiring board for a semiconductor device, comprising

a predetermined wiring section being disposed on an insulation board; and

an electromagnetic shielding film being placed at a position close to said wiring section,

wherein a distance defined between said wiring section and said electromagnetic shielding film is 150 μm or less and a volume specific resistance of said electromagnetic shielding film is 30 μΩ·cm or less at room temperature, and

wherein, over an applicable frequency between about 10 MHz to 15GHz, an inductance of said wiring section and inductive cross talk are reduced.

5. (Amended) A circuit board for electronic parts, comprising:

a plate-like ground layer;

an insulating substrate disposed on said plate-like ground layer;

[a circuit board prepared by forming] a plurality of leads disposed on [an] the insulating [material] substrate; and

a conductor disposed on an insulating material on said plurality of leads,

wherein said conductor disposed on said insulating material on said plurality of leads reduces a self inductance of said plurality of leads by flowing eddy current through said [plate-like] conductor, and

wherein said insulating substrate disposed on said plate-like ground layer reduces a self inductance of said plurality of leads by flowing eddy current through said plate-like ground layer.

6. (Amended) The circuit board for electronic parts as claimed in claim 5, wherein [said insulation board being formed on a ground layer decreasing a self inductance of said plurality of leads by flowing said eddy current through said conductor; and]

said conductor [forming] forms a composite sheet together with said insulating material.

IN THE ABSTRACT OF THE DISCLOSURE:

Please replace the entire Abstract of The Disclosure on page 37 with the following paragraph:

--A wiring board for a semiconductor device includes a wiring section disposed on an insulation board and an electromagnetic shielding film disposed at a position close to the wiring section. A distance defined between the wiring section and the electromagnetic shielding film is 150 μm or less and a volume specific resistance of said electromagnetic shielding film is 30 μΩ·cm or less at a room temperature. This structure reduces an inductance of the wiring section and inductive cross talk at frequencies between about 10 MHz to 15GHz. A circuit board for electronic parts is also provided including a plate-like ground layer, an insulating substrate disposed on the plate-like ground layer, a plurality of leads disposed on the insulating substrate, and a conductor disposed on an insulating material on the plurality of leads. The conductor disposed on

the insulating material on the plurality of leads reduces a self inductance of the plurality of leads by flowing eddy current through the conductor and the insulating substrate disposed on the plate-like ground layer reduces a self inductance of the plurality of leads by flowing eddy current through the plate-like ground layer.--